from a predetermined plurality of memory cells in response to a read mode command incorporated in synchronization with said clock signal each for successively transferring said data to a corresponding data output [terminals] terminal in response to said clock signal;

a plurality of compression means each provided corresponding to [each] a respective read means for carrying out a prescribed logical operation on said data read by a corresponding read means from said predetermined plurality of memory cells thereby compressing said data to one-bit data; and

output means for generating outputs of each respective compression means to said corresponding data output [terminals] terminal.

---

4. (Twice Amended) A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of banks each having a memory cell array;

activation means provided for the plurality of banks for activating and precharging [the] each memory [arrays] array of said plurality of banks on a bank by bank basis;

a data output terminal provided in common for said plurality of banks;

101

read means provided for each of said plurality of banks for simultaneously reading data from a predetermined plurality of memory cells [from a corresponding] <u>of the</u> memory cell array <u>corresponding to one of said plurality of banks</u> in response to a read mode command incorporated in synchronization with said clock signal for successively transferring said data to said data output terminal in response to said clock signal;

a plurality of first compression means provided corresponding to the banks and each said first compression means for carrying out a prescribed logical operation on said data read by corresponding read means from said plurality of memory cells in an activated bank for compressing said data to one-bit data; and

second compression on outputs for carrying out another prescribed logical operation on outputs of said plurality of first compression means for compressing said outputs to one-bit data and externally outputting the same to said data output terminal.

5. (Twice Amended) A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of banks each having a memory cell array;

activation means provided corresponding to the banks and for activating and precharging corresponding memory arrays, on a bank

102

by bank basis;

a plurality of data output terminals shared by said plurality of banks;

Cont. 1 B8

a plurality of read means provided corresponding to said plurality of data output terminals in each said bank for simultaneously reading data from a predetermined plurality of memory cells [from a corresponding] of the memory cell array corresponding to one of said plurality of banks in response to a read mode command incorporated in synchronization with said clock signal for successively transferring said data to [corresponding] said plurality of data output terminals in response to said clock signal;

a plurality of first compression means provided corresponding to the respective banks for carrying out a first logical operation on said data read by each of said plurality of read means from said predetermined plurality of memory cells in each said bank for compressing said data to one-bit data; and

second compression means for carrying out a second logical operation on outputs of said plurality of first compression means for compressing said outputs to one-bit data and externally outputting the same.

Claim 9, line 7 (of amendment filed March 31, 1995), delete "with each memory cell array".

103